AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A semiconductor device comprising:

a clock input terminal for receiving an input clock signal;

a digital clock manager, comprising a plurality of series connected delay elements coupled to a multiplexer, for generating a plurality of clock signals in response to the input clock signal, wherein the plurality of clock signals are delayed versions of the input clock signal;

a plurality of input/output blocks, including a first set of IOBs configured to operate in response to a first clock signal of the plurality of clock signals, a second set of IOBs configured to operate in response to a second clock signal of the plurality of clock signals, and a third set of IOBs configured to operate in response to a third clock signal of the plurality of clock signals.

2. (Original) The semiconductor device of Claim 1, wherein the first clock signal is synchronous with the input clock signal, the second clock signal is delayed by a phase angle of 90 degrees with respect to the first clock signal, and the third clock signal is delayed by a phase angle of 180 degrees with respect to the first clock signal.

3. (Original) The semiconductor device of Claim 1, wherein each of the plurality of clock signals is delayed by a predetermined phase with respect to the input clock signal.

4. (Original) The semiconductor device of Claim 1, wherein the first, second and third sets of IOBs are interleaved along a perimeter of the semiconductor device.

5. (Previously Presented) The semiconductor device of Claim 1, wherein the plurality of input/output blocks further includes a fourth set of IOBs configured to operate in response to a fourth clock signal of the plurality of clock signals.

6. (Original) The semiconductor device of Claim 1, wherein each of the plurality of clock signals has the same frequency.

7. (Original) The semiconductor device of Claim 1, wherein each of the plurality of clock signals exhibits a rising edge during a single period of the input clock signal.

8. (Previously Presented) A method of operating a semiconductor device comprising:

receiving an input clock signal;

generating a plurality of clock signals in response to the input clock signal;

operating a first set of input/output blocks in response to a first clock signal of the plurality of clock signals, wherein the first clock signal lags the input clock signal by a predetermined first phase angle; and

operating a second set of input/output blocks in response to a second clock signal of the plurality of clock signals, wherein the second clock signal lags the input clock signal by a predetermined second phase angle.

Claims 9-10. (Cancelled)

11. (Previously Presented) The method of Claim 8, wherein the predetermined first phase angle is zero degrees and the second predetermined phase angle is 90 degrees.

12. (Previously Presented) The method of Claim 8, wherein the predetermined first phase angle is 90 degrees and the second predetermined phase angle is 180 degrees.

Claim 13. (Cancelled)

14. (Original) The method of Claim 8, wherein each of the plurality of clock signals has the same frequency.

15. (Original) The method of Claim 8, wherein each of the plurality of clock signals exhibits a rising edge during a single period of the input clock signal.

16. (Previously Presented) A method of operating a semiconductor device comprising:

determining a period of an input clock signal;

introducing a plurality of discrete delays to the input clock signal, thereby generating a corresponding plurality of delayed clock signals, wherein the sum of the delays is less than the period of the input clock signal; and

using the plurality of delayed clock signals to control output switching of the semiconductor device.

17. (Previously Presented) The method of Claim 16, wherein the step of determining the period of the input clock signal comprises:

applying the input clock signal to a delay line having a plurality of series-connected delay elements; and

selecting an output clock signal from the delay line such that the output clock signal is synchronized with the input clock signal.

18. (Previously Presented) The method of Claim 17, wherein a number of delay elements are introduced to the path of the input clock signal to create the output clock signal, wherein the number of delay elements introduce a signal delay corresponding with one period of the input clock signal and wherein the number is at least two.

19. (Previously Presented) The method of Claim 18, further comprising determining each of the plurality of discrete delays in response to the number of delay elements.

20. (Previously Presented) The method of Claim 19, wherein each of the plurality of discrete delays is determined by dividing the number of delay elements by the number of delayed clock signals.

21. (Previously Presented) A semiconductor device comprising:

a digital clock manager configured to identify a period of an input clock signal;

a plurality of series-connected programmable delay lines configured to provide a corresponding plurality of delayed clock signals in response to the input clock signal; and

delay control circuitry coupled to the digital clock manager and the programmable delay lines, wherein the delay control circuitry is configured to program a delay in each of the plurality of series-connected programmable delay lines in response to the period of the input clock signal.

22. (Original) The semiconductor device of Claim 21, wherein the digital clock manager comprises a delay select circuit configured to introduce delay elements to a path of the input clock signal to create a delayed clock signal, wherein the delay select circuit is configured to introduce delay elements such that the input clock signal is synchronized with the delayed clock signal.

23. (Previously Presented) The semiconductor device of Claim 22, wherein the delay control circuitry comprises an arithmetic unit configured to divide a number of delay elements introduced by the digital clock manager by a number of programmable delay lines.

24. (Original) The semiconductor device of Claim 21, wherein the digital clock manager comprises:

a delay line configured to receive the input clock signal, wherein the delay line includes a plurality of series-connected delay elements;

a selector circuit configured to receive delayed clock signals from the series-

connected delay elements, and route one of the delayed clock signals as an output clock signal in response to a delay select value; and

a delay select circuit configured to provide the delay select value to the selector circuit, wherein delay select circuit selects the delay select value such that the input clock signal is synchronous with the output clock signal.

25. (Previously Presented) The semiconductor device of Claim 24, wherein each of the series-connected programmable delay lines includes one or more delay elements that are identical to the series-connected elements of the delay line.

26. (Original) A semiconductor device comprising:

means for determining a period of an input clock signal;

means for introducing a plurality of delays to the input clock signal, thereby generating a corresponding plurality of delayed clock signals, wherein the sum of the delays is less than the period of the input clock signal; and

means for using the plurality of delayed clock signals to control output switching of the semiconductor device.